Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1 (currently amended): In a processor, a method for performing computer graphics ~~calculations~~ view volume clipping comparisons to determine if a vertex is located within a specified view volume, ~~said~~ the method comprising:

~~representing a vertex in a computer graphics image with a plurality of coordinates;~~

transforming ~~said~~ a plurality of coordinates representing the vertex into a plurality of transformed coordinates; and

using a floating point magnitude compare instruction to perform a magnitude comparison ~~of absolute values~~ between an absolute value of at least ~~a portion~~ one of ~~said~~ the plurality of transformed coordinates and an absolute [[a]] value that represents, for each respective at least one transformed coordinate, ~~representing a plurality of edges of a specified view volume~~ opposing view volume edges in the specified view volume in a dimension corresponding to the respective at least one transformed coordinate, wherein comparison results for at least ~~three~~ two view volume edges are obtained.

Claim 2 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ of Claim [[1]] 1, wherein ~~said portion~~ each of the at least one of ~~said~~ the plurality of transformed coordinates are processed in parallel.

Claim 3 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ of Claim [[1]] 1, further comprising:

setting a plurality of condition code bits to one or more specific states to indicate results of ~~said~~ the magnitude comparison.

Claim 4 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ of Claim [[1]] 1, further comprising:

specifying a compare condition in ~~said~~ the floating point magnitude compare instruction.

Claim 5 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ of Claim [[4]] 4, further comprising:

setting one of ~~said~~ the plurality of condition code bits to indicate true if an associated compare condition is true and setting ~~said~~ the one condition code bit to indicate false if ~~said~~ the associated compare condition is false.

Claim 6 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ of Claim [[1]] 1, further comprising:

converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction.

Claim 7 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ <u>of</u> Claim [[6]] <u>6,</u> wherein ~~said~~ <u>the</u> first convert instruction is a CVT.PS.PW instruction.

Claim 8 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ <u>of</u> Claim [[1]] <u>6,</u> further comprising:

converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction.

Claim 9 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ <u>of</u> Claim [[8]] <u>8,</u> wherein ~~said~~ <u>the</u> second convert instruction is a CVT.PW.PS instruction.

Claim 10 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ <u>of</u> Claim [[1]] <u>1,</u> wherein ~~said~~ <u>the</u> floating point magnitude compare instruction is a CABS instruction.

Claim 11 (currently amended): A ~~processor for computer graphics calculations, said processor comprising:~~

~~a bus;~~

~~an instruction dispatch unit coupled to said bus, said instruction dispatch unit for dispatching instructions to a floating point unit; and~~

~~said floating point unit coupled to said bus, said floating point unit for executing said instructions to implement a method~~ <u>system</u> that performs computer graphics ~~calculations~~ <u>view volume clipping comparisons to determine if a vertex is located within a specified view volume</u>, ~~said method~~ <u>the system</u> comprising:

~~representing a vertex in a computer graphics image with a plurality of coordinates;~~

<u>means for</u> transforming ~~said~~ <u>a</u> plurality of coordinates <u>representing the vertex</u> into a plurality of transformed coordinates; and

~~using a floating point magnitude compare instruction to perform~~ <u>means for performing</u> a magnitude comparison<u>, via a floating point magnitude compare instruction,</u> ~~of absolute values~~ between <u>an absolute value of</u> at least ~~a portion~~ <u>one</u> of ~~said~~ <u>the</u> plurality of transformed coordinates and <u>an absolute</u> [[a]] value<u> that represents, for each respective at least one transformed coordinate,</u> ~~representing a plurality of edges of a specified view volume~~ <u>opposing view volume edges in the specified view volume in a dimension corresponding to the respective at least one transformed coordinate</u>, wherein comparison results for at least ~~three~~ <u>two</u> view volume edges are obtained.

Claim 12 (currently amended): The ~~processor~~ system of Claim 11, further comprising:

~~wherein said method for performing computer graphics calculations further comprises:~~

means for setting a plurality of condition code bits to one or more specific states to indicate results of ~~said~~ the magnitude comparison.

Claim 13 (currently amended): The ~~processor~~ system of Claim 11, further comprising:

~~wherein said method for performing computer graphics calculations further comprises:~~

means for specifying a compare condition in ~~said~~ the magnitude compare instruction.

Claim 14 (currently amended): The ~~processor~~ system of Claim 13, further comprising:

~~wherein said method for performing computer graphics calculations further comprises:~~

means for setting one of ~~said~~ the plurality of condition code bits to indicate true if an associated compare condition is true and setting ~~said~~ the one condition code bit to indicate false if ~~said~~ the associated compare condition is false.

Claim 15 (currently amended): The ~~processor~~ system of Claim 11, further comprising:

~~wherein said method for performing computer graphics calculations further comprises:~~

means for converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction.

Claim 16 (currently amended): The ~~processor~~ system of Claim ~~15~~ 15, wherein ~~said~~ the first convert instruction is a CVT.PS.PW instruction.

Claim 17 (currently amended): The ~~processor~~ system of Claim [[11]] 15, further comprising: ~~wherein said method for performing computer graphics calculations further comprises:~~

means for converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction.

Claim 18 (currently amended): The ~~processor~~ system of Claim ~~17~~ 17, wherein ~~said~~ the second convert instruction is a CVT.PW.PS instruction.

Claim 19 (currently amended): The ~~processor~~ system of Claim ~~11~~ 11, wherein ~~said~~ the floating point magnitude compare instruction is a CABS instruction.

Claims 20-39 (canceled)

Claim 40 (currently amended): The method ~~for performing computer graphics calculations as recited in~~ of Claim [[1]] 1, wherein ~~said~~ the plurality of coordinates and ~~said~~ the plurality of transformed coordinates are in a paired-single data format.

Claim 41 (currently amended): The ~~processor~~ system of Claim ~~11~~ 11, wherein ~~said~~ the plurality of coordinates and ~~said~~ the plurality of transformed coordinates are in a paired-single data format.

Claim 42 (new): The method of Claim 1, wherein the floating point magnitude compare instruction is part of a general purpose instruction set architecture.

Claim 43 (new): The method of Claim 1, wherein the floating point magnitude compare instruction is part of an application specific extension to a general purpose instruction set architecture.

Claim 44 (new): The method of Claim 1, wherein the floating point magnitude compare instruction is executed in a single clock cycle.

Claim 45 (new): The system of Claim 11, wherein the means for performing includes means for processing each of the at least one of the plurality of transformed coordinates in parallel.

Claim 46 (new): The system of Claim 11, wherein the floating point magnitude compare instruction is part of a general purpose instruction set architecture.

Claim 47 (new): The system of Claim 11, wherein the floating point magnitude compare instruction is part of an application specific extension to a general purpose instruction set architecture.

Claim 48 (new): The system of Claim 11, wherein the floating point magnitude compare instruction is executed in a single clock cycle.